**Timer Module Verification Results**

TCL Output:

TIMER\_TC\_01: PASS

TIMER\_TC\_02: PASS

TIMER\_TC\_03: PASS

TIMER\_TC\_04: PASS

INFO: [USF-XSim-96] XSim completed. Design snapshot 'rtc\_timer\_tb\_behav' loaded.

INFO: [USF-XSim-97] XSim simulation ran for 1000ns

launch\_simulation: Time (s): cpu = 00:00:06 ; elapsed = 00:00:08 . Memory (MB): peak = 885.027 ; gain = 13.770

run 100 ms

TIMER\_TC\_05: PASS

TIMER\_TC\_06: PASS

TIMER\_TC\_07: PASS

TIMER\_TC\_08: PASS

TIMER\_TC\_09:

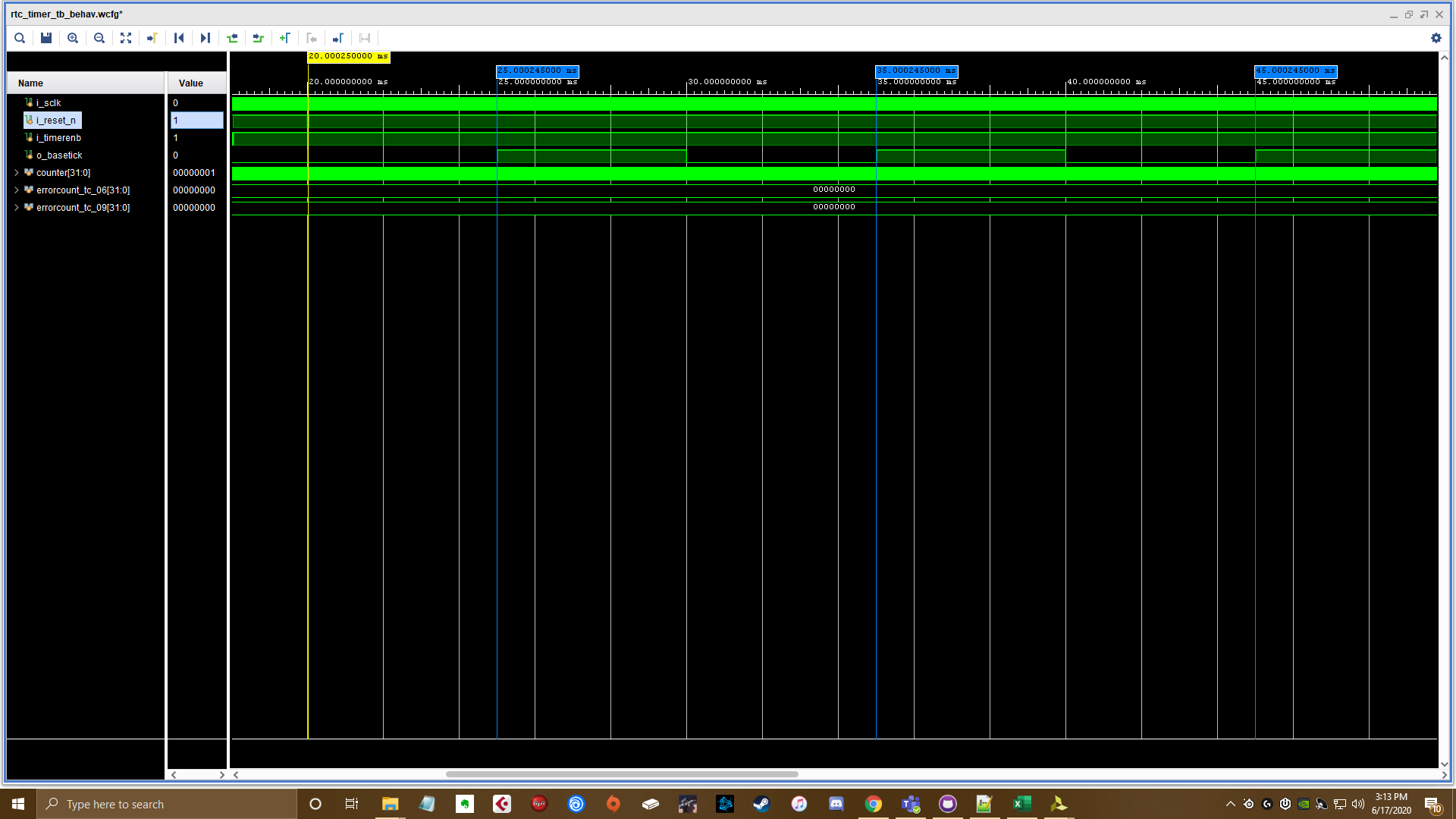
Start time: 20000250000

VERIFY TIMER\_TC\_09 BY OBSERVATION.

o\_basetick should show a 10ms period after start time.

run: Time (s): cpu = 00:00:28 ; elapsed = 00:00:27 . Memory (MB): peak = 898.375 ; gain = 6.945

TIMER\_TC\_09: Verified through observation



* Waveform shows 10ms period output on ‘o\_basetick’ after test case start time.